AN1723
APPLICATION NOTE

DESIGNING WITH L5973AD, UP TO 2A HIGH EFFICIENCY DC/DC CONVERTER

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L5973AD INTRODUCTION

The L5973AD is a step down monolithic power switching regulator capable to deliver up to 2A at output voltages from 1.235V to 35V. The operating input voltage ranges from 4.4V to 36V. It is realized in BCDV technology and the power switching element is realised by a P-Channel D-MOS transistor. It doesn't require a bootstrap capacitor, and the duty cycle can range up to 100%.

An internal oscillator fixes the switching frequency at 500KHz. This minimizes the LC output filter.

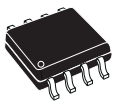
Synchronization pin is available in the case higher frequency is requested.

Pulse by pulse and frequency foldback overcurrent protections offer an effective short circuit protection.

Other features are voltage feed forward, protection against feedback disconnection, inhibit and thermal shutdown.

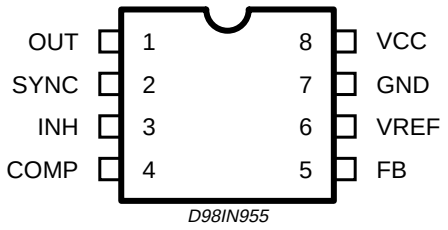
The device is housed in an HSOP8 package with exposed pad that helps to reduce the thermal resistance Junction to Ambient (R_{Thj-a}) down to approximately 40°C/W.

Figure 1. Package



HSOP8 - Exposed Pad

Figure 2. Pins connection



PINS FUNCTIONS

N.	Name	Description
1	OUT	Regulator Output.
2	SYNC	Master/Slave Synchronization. When it is open, a signal synchronous with the turn-off of the internal power is present at the pin. When connected to an external signal at a frequency higher than the internal one, then the device is synchronized by the external signal. Connecting together the SYNC pin of two devices, the one with the higher frequency works as master and the other one, works as slave.
3	INH	A logical signal (active high) disables the device. With IHN higher than 2.2V the device is OFF and with INH lower than 0.8V, the device is ON. If INH is not used the pin must be grounded. When it is open, an internal pull-up disables the device.
4	COMP	E/A output to be used for frequency compensation.
5	FB	Stepdown feedback input. Connecting the output voltage directly to this pin results in an output voltage of 1.235V. An external resistor divider is required for higher output voltages (the typical value for the resistor connected between this pin and ground is 4.7K).
6	V_{REF}	Reference voltage of 3.3V. No filter capacitor is needed to stability.
7	GND	Ground.
8	V_{CC}	Unregulated DC input voltage.

APPLICATION INFORMATION:

In figure 3 is shown the demo board application circuit, where the input supply voltage, Vcc, can range from 4.4V to 25V due to the rated voltage of the input capacitor and the output voltage is adjustable from 1.235V to V_{cc}.

Figure 3. Demo board Application Circuit

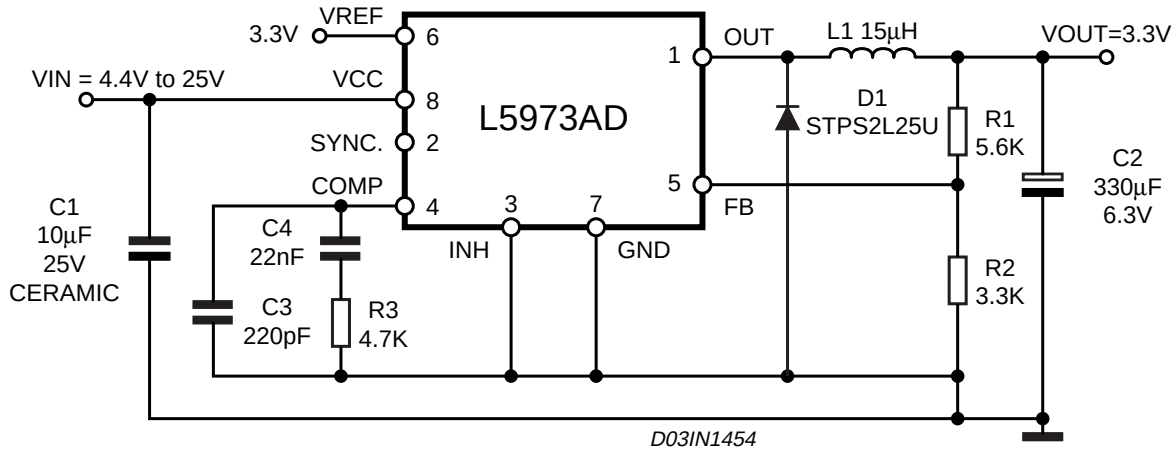


Table 1. Component List

Reference	Part Number	Description	Manufacturer
C1		10µF, 25V	TOKIN
C2	POSCAP 6TPB330M	330µF, 6.3V	Sanyo
C3	C1206C221J5GAC	220pF, 5%, 50V	KEMET
C4	C1206C223K5RAC	22nF, 10%, 50V	KEMET
R1		5.6K, 1%, 0.1W 0603	Neohm
R2		3.3K, 1%, 0.1W 0603	Neohm
R3		4.7K, 1%, 0.1W 0603	Neohm
D1	STPS2L25U	2A, 25V	ST
L1	DO3316P-153	15µH, 3A	COILCRAFT

Figure 4. PCB layout (component side)

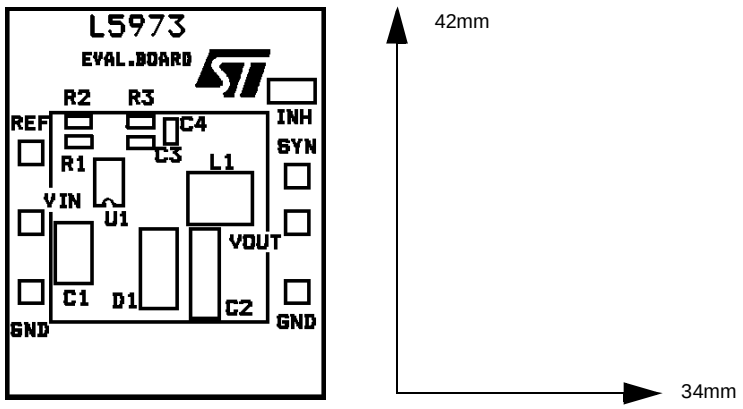


Figure 5. PCB layout (bottom side)

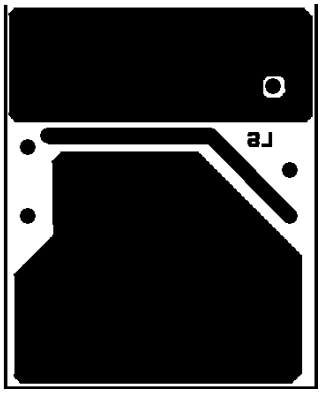
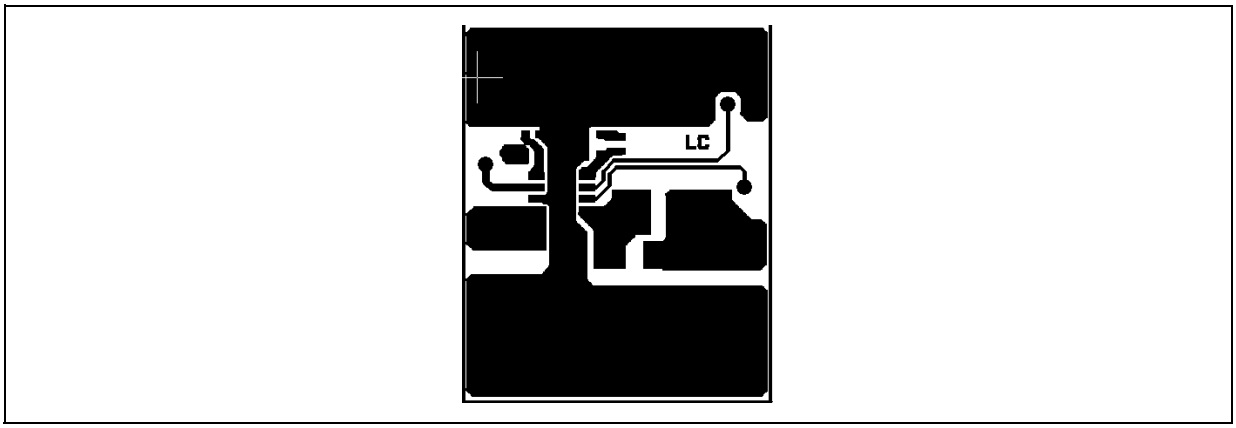


Figure 6. PCB layout (front side)



Below some graphs show the Tj versus output current in different conditions of the input and output voltage and some efficiency measurements.

Figure 7. Junction Temperature vs. Output Current

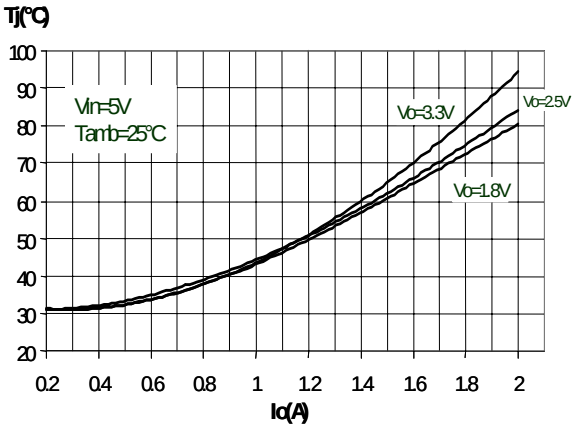


Figure 8. Junction Temperature vs Output Current

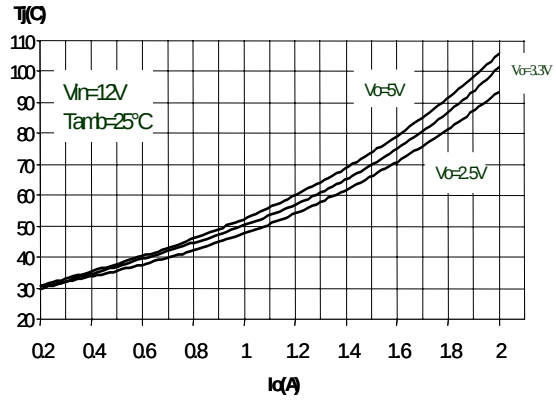


Figure 9. Efficiency vs. Output Current

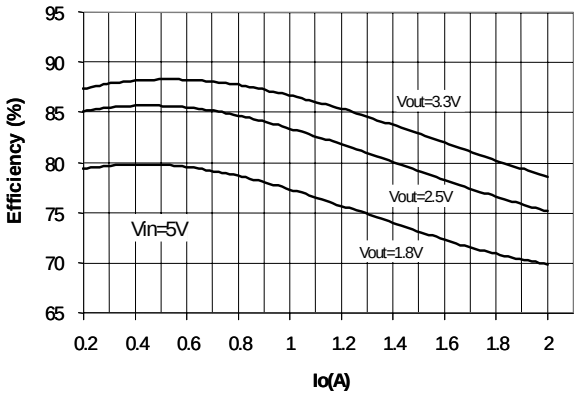
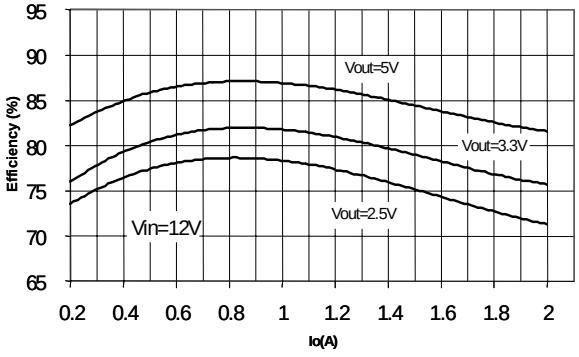


Figure 10. Efficiency vs. Output Current



The following points will be analysed .

1.0 Components Selection

2.0 Closing the Loop

3.0 Layout Consideration

3.1 Thermal Considerations

3.2 Shortcircuit Protection

4.0 Application Ideas

1.0 COMPONENTS SELECTION

1.1 Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current that can be up to the load current divided by two (worst case, with duty cycle of 50%).

For this reason, the quality of these capacitors has to be very high to minimize its power dissipation generated by the internal ESR, so improving the system reliability and efficiency.

The critical parameter is usually the RMS current rating that has to be higher than the RMS input current.

The maximum RMS input current (flowing through the input capacitor) is:

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta}}$$

Where η is the expected system efficiency, D is the duty cycle and Io the output DC current. This function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to I_O divided by 2 (considering η = 1).

The maximum and minimum duty cycles are:

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}} \qquad \text{and} \qquad D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

Where V_F is the freewheeling diode forward voltage and V_{SW} the voltage drop across the internal PDMOS. Considering the range D_{MIN} to D_{MAX} it is possible to determine the max I_{RMS} following through the input capacitor. Different capacitors can be considered:

- Electrolytic Capacitors.

  These are the most used cause are the cheapest ones and are available with a wide range of RMS current ratings. The only drawback is that, considering a requested ripple current rating, they are physically larger than other capacitors.

- Ceramic Capacitors.

  If available for the requested value and voltage rating, these capacitors have usually an higher RMS current rating for a given physical dimension (due to the very low ESR). The drawback is the quite high cost.

- Tantalum Capacitor.

  Very good tantalum capacitors are coming available, with very low ESR and small size. The only problem is that they occasionally can burn if subjected to very high current during the charge. So, it is better avoid this type of capacitors for the input filter of the device. Infact, they can be subjected to high surge current when connected to the power supply.

1.2 Output capacitor

The output capacitor is very important to satisfy the output voltage ripple requirement.

Using a small inductor value is useful to reduce the size of the choke but increases the current ripple. So, to reduce the output voltage ripple a low ESR capacitor is required. Nevertheless, the ESR of the output capacitor introduces a zero in the open loop gain, that helps to increase the phase margin of the system. If the zero goes at very high frequency, its effect is negligible. For this reason, ceramic capacitors and very low ESR capacitors in general should be avoided.

Tantalum and electrolytic capacitors are usually good for this use.

Below there is a list of some tantalum capacitors manufacturer.

Table 2.

Manufacturer	Series	Cap Value (µF)	Rated Voltage (V)	ESR (mΩ)
AVX	TPS	100 to 470	4 to 35	50 to 200
KEMET	T494/5	100 to 470	4 to 20	30 to 200
SANYO POSCAP(*)	TPA/B/C	100 to 470	4 to 16	40 to 80
SPRAGUE	595D	220 to 390	4 to 20	160 to 650

(*) POSCAP capacitors have characteristic very similar to tantalum ones.

1.3 Inductor

The inductor value is very important cause it fixes the ripple current flowing through output capacitor.

The ripple current is usually fixed at 20-40% of Iomax, that is 0.3-0.6A with Iomax = 1.5A. The inductor value is approximately obtained by the following formula:

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I} \cdot T_{ON}$$

where T_{on} is the ON time of the internal switch, given by $D \cdot T$.

For example, with V_{OUT} = 3.3V, V_{IN} = 12V and ΔI_O = 0.45A, the minimum inductor value is about 12µH.

The peak current thought the inductor is given by:

$$I_{PK} = I_O + \frac{\Delta I}{2}$$

and it can be seen that if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. So, fixed the peak current, higher value of the inductor permit higher value for the output current.

In the following table some inductor manufacturer are listed.

Table 3.

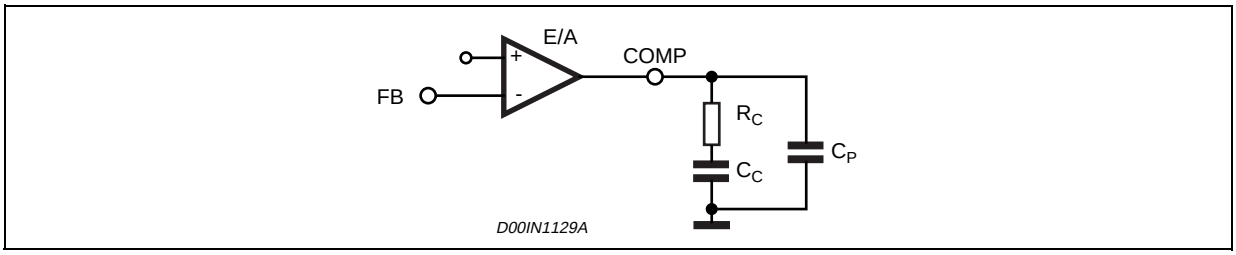
Manufacturer	Series	Inductor Value (µH)	Saturation Current (A)
Coilcraft	DO3316	15 to 33	2.0 to 3.0
Coiltronics	UP1B	22 to 33	2.0 to 2.4
BI	HM76-3	15 to 33	2.5 to 3.3
Epcos	B82476	33 to 47	1.6 to 2
Wurth Elektronik	744561	33 to 47	1.6 to 2

2.0 CLOSING THE LOOP

2.1 Compensation Network

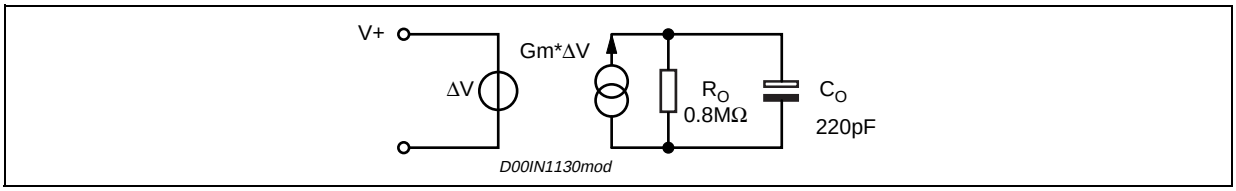
The output L-C filter of a step down converter contributes with 180 degrees phase shift in the control loop. For this reason a compensation network between the COMP pin and ground is added. The simplest loop compensation network is shown in fig. 11. R_C and C_C introduce a pole and a zero in the open loop gain. C_P doesn't affect really the system stability but is useful to reduce the noise of the COMP pin.

Figure 11. Compensation Network



The equivalent circuit of the error amplifier is shown in fig.12

Figure 12. Error Amplifier Equivalent Circuit



Considering R_C = 4.7kΩ, C_C = 22nF and C_P = 220pF (see fig. 3), the transfer function $A_o(s)$ of the error amplifier and its compensation network becomes:

$$A_o(s) = \frac{A_{vo} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_o \cdot (C_o + C_p) \cdot R_c \cdot C_c + s \cdot (R_o \cdot C_c + R_o \cdot (C_o + C_p) + R_c \cdot C_c) + 1}$$

Where $A_{vo} = G_m \cdot R_o$

The poles and zeroes of this transfer function are:

$$F_{P1} = \frac{1}{2 \cdot \pi \cdot R_o \cdot C_c} = \frac{1}{2 \cdot \pi \cdot [0.8 \cdot 10^6] \cdot 22 \cdot 10^{-9}} = 9Hz$$

$$F_{P2} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_o + C_p)} = \frac{1}{2\pi \cdot 4.7 \cdot 10^3 \cdot 220 \cdot 10^{-12}} = 154kHz$$

$$F_{Z1} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c} = \frac{1}{2\pi \cdot 4.7 \cdot 10^3 \cdot 22 \cdot 10^{-9}} = 1.5kHz$$

Fp1 is the low frequency pole that sets the bandwidth while the zero Fz1 is usually put near to the frequency of the double pole of the L-C filter (see below). Fp2 is usually at a very high frequency.

The transfer function of the L-C filter is given by:

$$A_{LC}(s) = \frac{1 + ESR \cdot C_{OUT} \cdot s}{L \cdot C_{OUT} \cdot s^2 + ESR \cdot s + 1}$$

The poles and zeroes of this transfer function are:

$$F_{PLC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}} = \frac{1}{2\pi \cdot \sqrt{15 \cdot 10^{-6} \cdot 330 \cdot 10^{-6}}} = 2.2kHz$$

$$F_o = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{OUT}} = \frac{1}{2\pi \cdot 0.08 \cdot 330 \cdot 10^{-6}} = 6kHz$$

Fo is the zero introduced by the ESR of the output capacitor and it is very important to increase the phase margin of the control loop. F_{pLC} is the double pole of the L-C filter.

The PWM gain is given by the following formula:

$$G_{PWM}(s) = \frac{V_{cc}}{(V_{OSCMAX} - V_{OSCMIN})}$$

Where $VOSC_{MAX}$ is the maximum value of a sawtooth waveform and $VOSC_{MIN}$ is the minimum one. A voltage feed forward is realized to have G_{PWM} constant. This feature is obtained generating a sawtooth waveform directly proportional to the input voltage V_{CC}.

$$V_{OSCMAX} - V_{OSCMIN} = K \cdot V_{CC}$$

Where K is equal to 0.076.

Therefore the PWM gain is also equal to

$$G_{PWM}(s) = \frac{1}{K} = Const$$

This means that also if the input voltage changes, the error amplifier doesn't change its value to keep the loop in regulation, so ensuring a better line regulation and line transient response.To sum up the Open Loop Gain can be written as:

$$G(s) = G_{PWM}(s) \cdot \frac{R_2}{R_1 + R_2} \cdot A_o(s) \cdot A_{LC}(s)$$

The Gain and Phase Bode are plotted in figures 13 and 14.

Figure 13. Module Plot

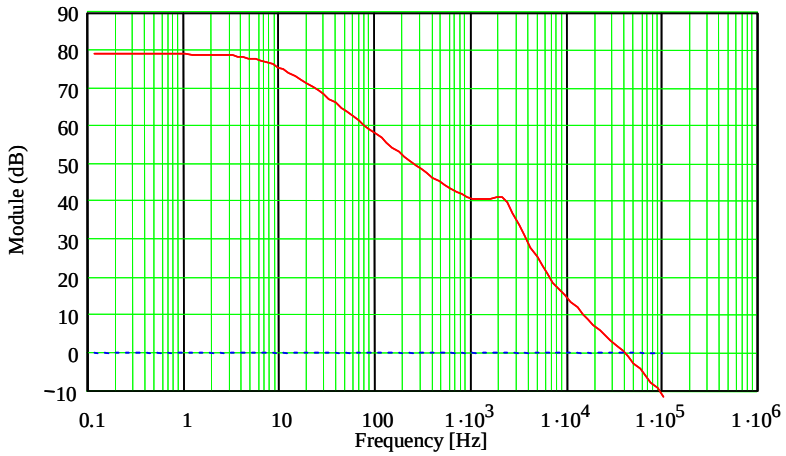
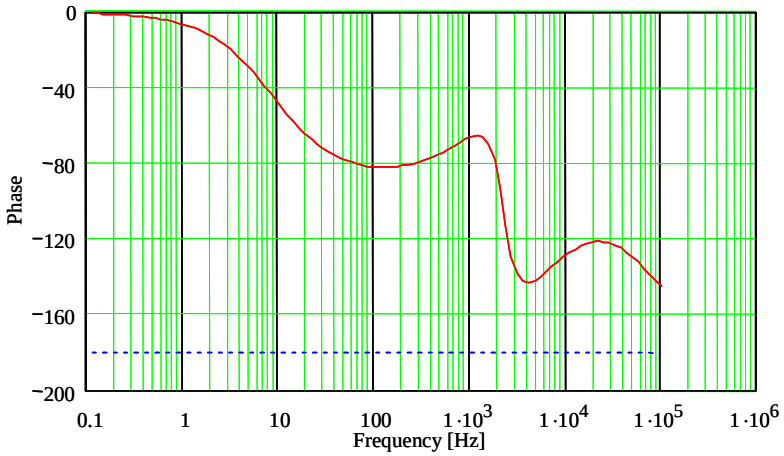


Figure 14. Phase Plot



The cut off frequency and the phase margin are:

F_C = 39KHz Phase Margin = 54°

3.0 LAYOUT CONSIDERATIONS

The layout of switching DC/DC converters is very important to minimize noise and interference.

Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference and so they should be as far as possible from the high current paths.

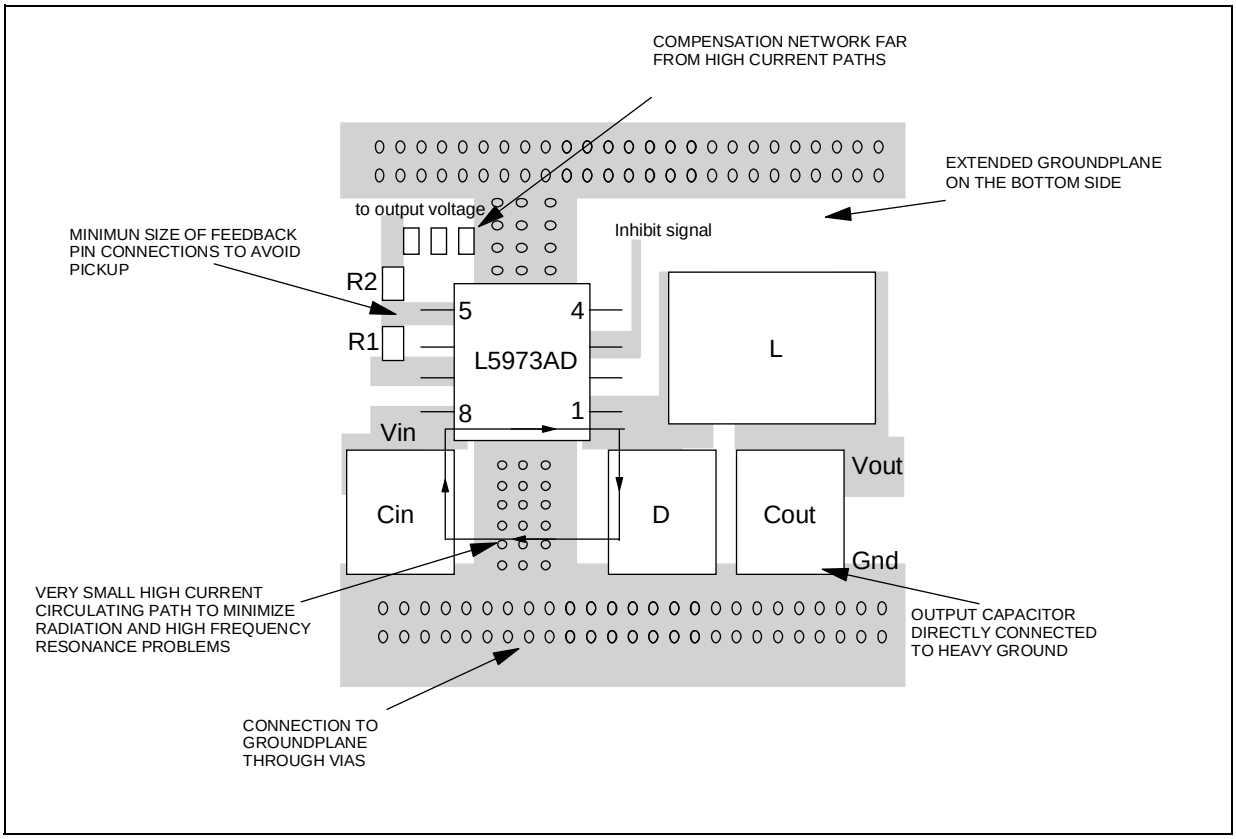
Below there is a layout example (Fig. 15).

The input and output loops are minimized to avoid radiation and high frequency resonance problems.

The feedback pin connections to the external divider are very close to the device to avoid pick up noise.

Another important issue is the groundplane of the board. Since the package has an exposed pad, it is very important to connect it to an extended groundplane in order to reduce the thermal resistance junction to ambient.

Figure 15. Layout example



3.1 THERMAL CONSIDERATIONS

The dissipated power of the device is related to three different sources:

- switch losses due to the not negligible R_{DSON}. These are equal to:

$$P_{ON} = R_{DSON} \cdot (I_{OUT})^2 \cdot D$$

Where D is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between Vout and Vin, but in practical is quite higher than this value to compensate the losses of the overall application. Due to this reason, the switch losses related to the R_{DSON} increases compared with the ideal case.

- Switch losses due to its Turn On and Off. These are given by the following relation:

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{ON} + T_{OFF})}{2} \cdot F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW}$$

Where T_{ON} and T_{OFF} are the overlap times of the voltage across the power switch and the current flowing into it during the Turn On and Turn Off phases. T_{SW} is the equivalent switching time.

- Quiescent current losses.

$$P_Q = V_{IN} \cdot I_Q$$

Where I_Q is the quiescent current.

Example:

Vin = 5V

Vout = 3.3V

Iout = 1.5A

R_{DSON} has a typical value of 0.25Ω @ 25°C and increases up to a maximum value of 0.5Ω @ 150°C. We can consider a value of 0.4Ω.

T_{SW} is approximately 70ns.

I_Q has a typical value of 5mA @ V_{in} = 12V.

The overall losses are:

$$P_{TOT} = R_{DSON} \cdot (I_{OUT})^2 \cdot D + V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW} + V_{IN} \cdot I_Q =$$

$$= 0.4 \cdot 1.5^2 \cdot 0.7 + 5 \cdot 1.5 \cdot 70 \cdot 10^{-9} \cdot 500 \cdot 10^3 + 5 \cdot 5 \cdot 10^{-3} \cong 0.9W$$

The junction temperature of device will be:

$$T_J = T_A + Rth_{J-A} \cdot P_{TOT}$$

Where T_A is the ambient temperature and Rth_{J-A} is the thermal resistance junction to ambient.

Considering that the device in mounted on board with a good groundplane has a thermal resistance junction to ambient (Rth_{J-A}) of about 42°C/W and considering an ambient temperature of about 70°C

$$T_J = 70 + 0.9 \cdot 42 \cong 108°C$$

3.2 SHORTCIRCUIT PROTECTION

In overcurrent protection mode, when the peak current reaches the current limit, the device reduces the Ton down to its minimum value (approximately 250nsec) and the switching frequency to approximately one third of its nominal value (see datasheet in the Current protection section).

In these conditions, the duty cycle is strongly reduced and, in most of the applications, this is enough to limit the current to Ilim. Anyway, in case of heavy short-circuit at the output (Vout=0V) and depending on the application conditions (Vcc value and parasitic effect of external components) the current peak could reach values higher than Ilim.

This can be understood considering the inductor current ripple during the ON and OFF phases:

ON Phase

$$\Delta I_L = \frac{(V_{IN} - V_{out} - DCR_L \cdot I)}{L} \cdot T_{ON}$$

OFF Phase

$$\Delta I_L = \frac{(V_D + V_{out} + DCR_L \cdot I)}{L} \cdot T_{OFF}$$

where V_D is the voltage drop across the diode and DCR_L is the series resistance of the inductor.

In shortcircuit conditions V_{OUT} is negligible. So, during the Toff, the voltage applied to the inductor is very small

and it can be that the current ripple in this phase does not compensate for the current ripple during the Ton.

The maximum current peak can be easily measured through the inductor with V_{out} = 0V (short-circuit) and V_{CC}=V_{inmax}. In case the application has to sustain the short-circuit condition for a long time, the external components (mainly inductor and diode) must be selected based on this value.

Figure 16. Shortcircuit Current. V_{IN} = 25V

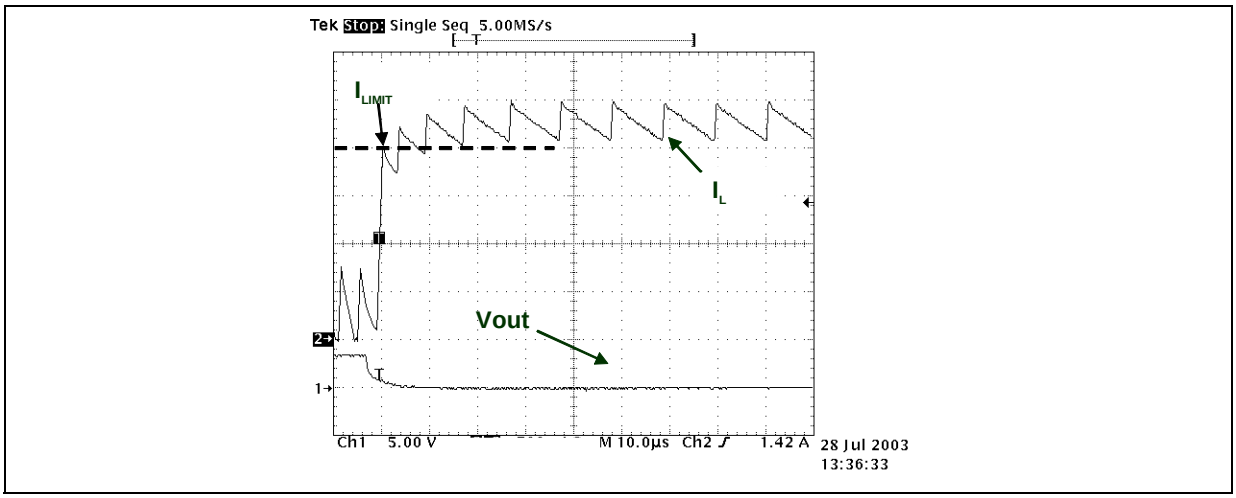
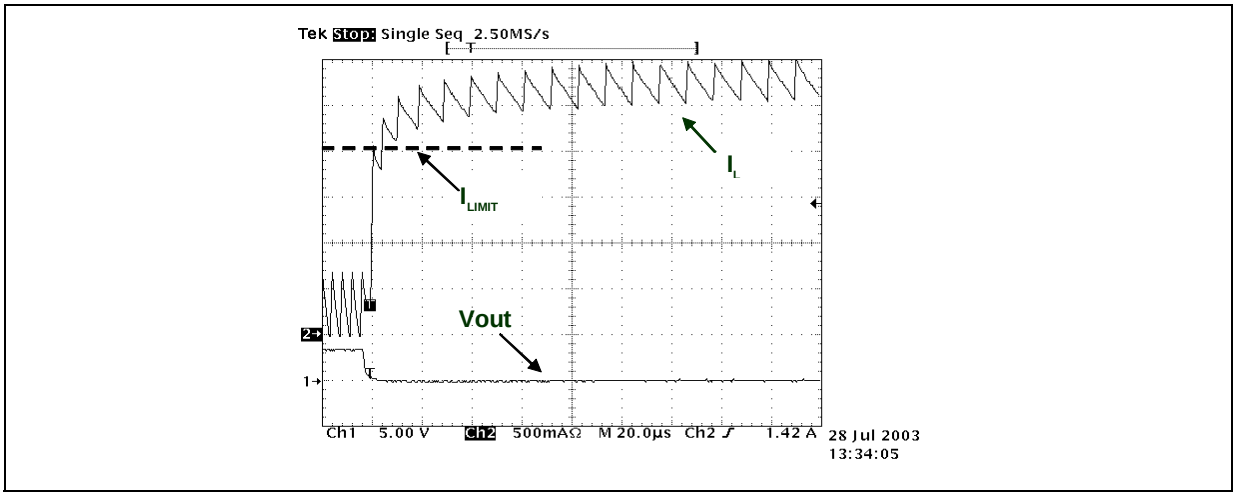


Figure 17. Shortcircuit Current. V_{IN} = 30V



As an example, in Fig16 and 17 it can be seen that, for a given component list, increasing the input voltage the current peak increases too. The current limit is immediately triggered but the current peak increases until the current ripple during the Toff is equal to the current ripple during the Ton.

4.0 APPLICATION IDEAS

4.1 POSITIVE BUCK-BOOST REGULATOR

The device can be used to realize an Up-Down converter with a positive output voltage. In figure 18 is shown the schematic circuit of this topology for an output voltage of 12V.

The input voltage can range from 5V and 35V.

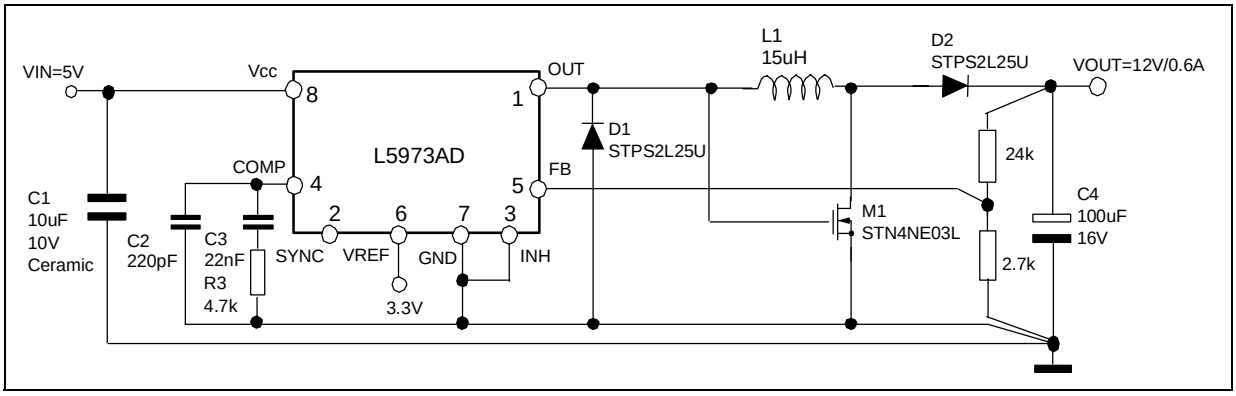
The output voltage is given by Vo = Vin · D/(1-D), where D is duty cycle.

The maximum output current is given by Iout = 1 x (1-D).

The current capability is reduced by the term (1-D) and so, for example, with a duty cycle of 0.5, and considering on average current following through the switch of 1.5A, the maximum output current deliverable to the load is 0.75A.

This is due to the fact that the current flowing trough the internal power switch is delivered to the output only during the OFF phase.

Figure 18. Positive Buck-Boost regulator



4.2 BUCK-BOOST REGULATOR

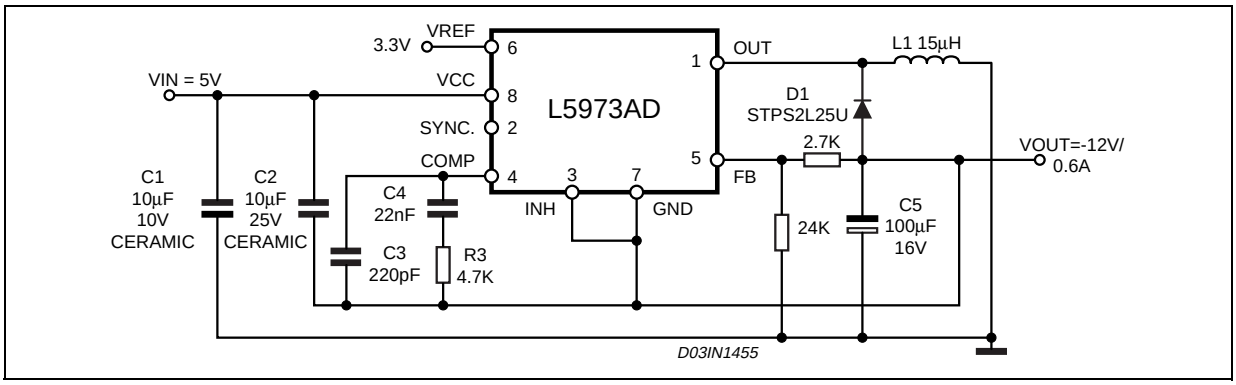
In Figure 19 is shown the schematic circuit to realize a standard Buck-Boost topology.

The output voltage is given by Vo=-Vin · D/(1-D).

The maximum output current is equal to Iout=1 · (1-D), for the same reason of the Up-Down converter.

An important thing to take in account is that the Gnd pin of the device is connected to the negative output voltage. So, the device undergoes a voltage equal to Vin-Vo, that has to be lower than 36V (maximum operating input voltage).

Figure 19. Buck-Boost regulator



4.3 DUAL OUTPUT VOLTAGE WITH AUXILIARY WINDING

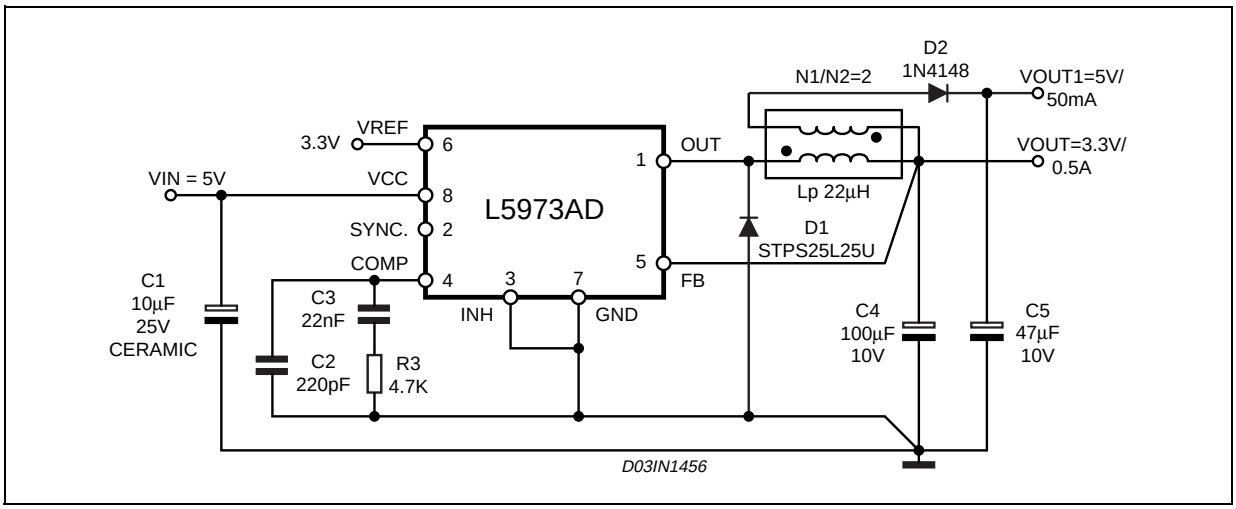
When two output voltages are required, it is possible to realize a dual output voltage converter by using a coupled inductor.

During the ON phase the current is delivered to Vout while D2 is reverse biased.

During the OFF phase the current is delivered, through the auxiliary winding, to the output voltage Vout1.

This is possible only if the magnetic core has stored a sufficient energy. So, to be sure that the application is working properly, the load related to the second output Vout1 should be much lower than the load related to Vout.

Figure 20. Dual output voltage with auxiliary winding

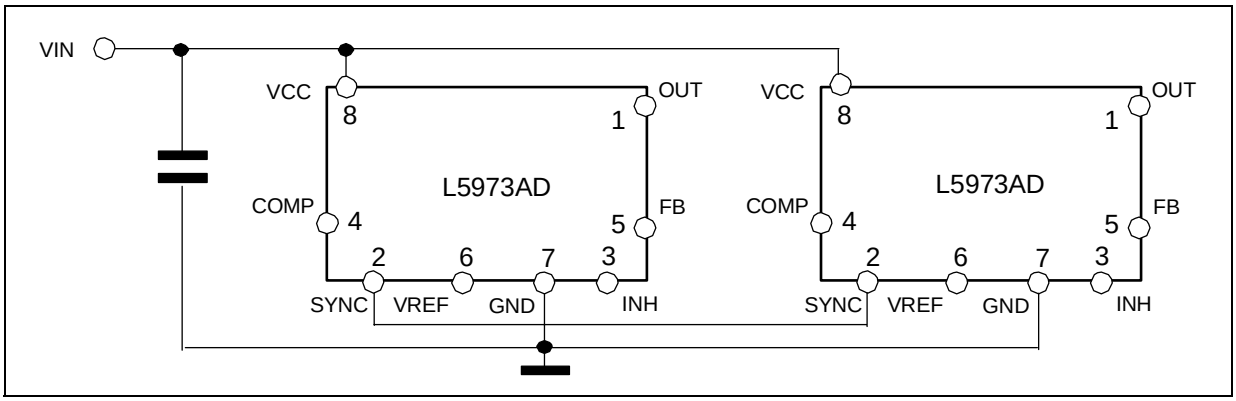


4.4 SYNCHRONIZATION EXAMPLE

Two or more devices (up to 6) can be synchronized just connecting together the synchronization pin. In this case, the device with an slightly higher switching frequency value will work as master and the ones with a slightly lower switching frequency value will work as a slave.

The device can also be synchronized from an external source. In this case the logic signal (see synchronization section) must have a frequency higher than the internal switching frequency of the device (500KHz).

Figure 21. Synchronization example



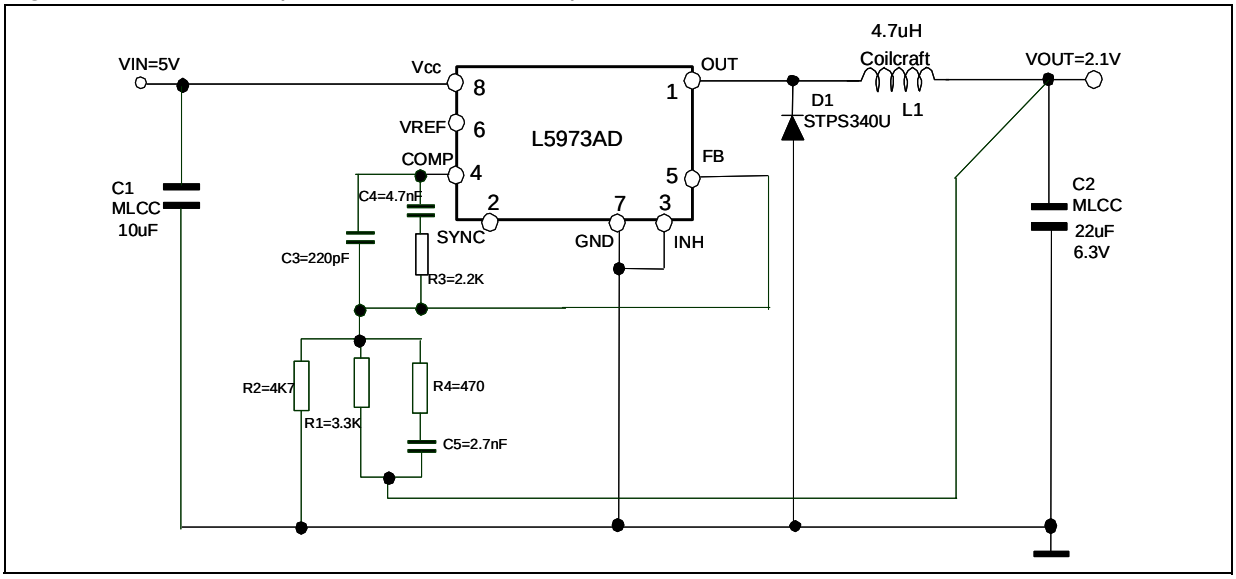
4.5 COMPENSATION NETWORK WITH MLCC (Multiple Layer Ceramic Capacitor) AT THE OUTPUT

MLCC with values in the range of 10uF-22µF and rated voltages in the range of 10V-25V are today available at relatively low cost from many manufacturers.

These capacitors have very low ESR values (few mohms) and so, sometimes, they are used for the output filter in order to reduce the voltage ripple and the overall size of the application.

However, the very low ESR value is affecting the compensation of the loop (see Section 2.0) and in order to keep the system stable, a more complicated compensation network could be required. Fig.22 shows and example of compensation network that makes the system stable with ceramic capacitors at the output (the optimum components value depends on the application).

Figure 22. MLCC: compensation network example



4.6 EXTERNAL SOFT START NETWORK

At the start up, the device can quickly increase the current up to the current limit in order to charge the output capacitor. In case a soft ramp up of the output voltage is required, an external soft start network can be implemented as shown in Fig.23.

The capacitor C is charged up to an external reference (through R) and the BJT clamps the COMP pin. This clamps the duty cycle, limiting the slew rate of the output voltage.

Figure 23. Soft Start Network Example